Ch2: Semiconductor Electronics – Part 2

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Junction Field-Effect Transistor (JFET)

Field-Effect Transistor (FET)

Field-Effect Transistors (**FETs**) or **Unipolar Transistors** operates similar to BJTs but on a **different principle**. A FET is a three terminal (namely **Drain**, **Source**, and **Gate**) semiconductor device in which current conduction is by **only one type** of charge carriers (electrons for n-channel type or holes for p-channel type).

Two main types of FETs:
(1) Junction Field-Effect Transistor (**JFET**),
(2) Metal-Oxide-Semiconductor FET (**MOSFET**) or Insulated Gate FET (**IGFET**).
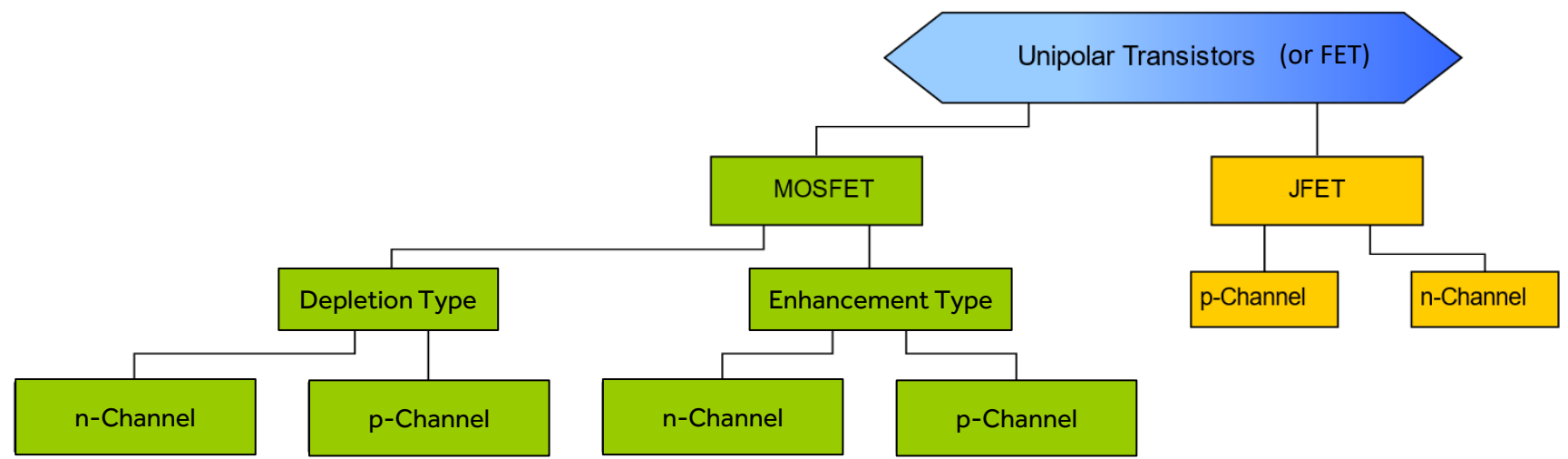
How a JFET Works

Junction Field-Effect Transistors (JFETs) come in either n-channel or p-channel configurations. An n-channel JFET is made with an n-type silicon channel that contains two p-type silicon "bumps" placed on either side. The **gate** lead is connected to the p-type bumps, while the **drain** and **source** leads are connected to either end of the n-type channel.
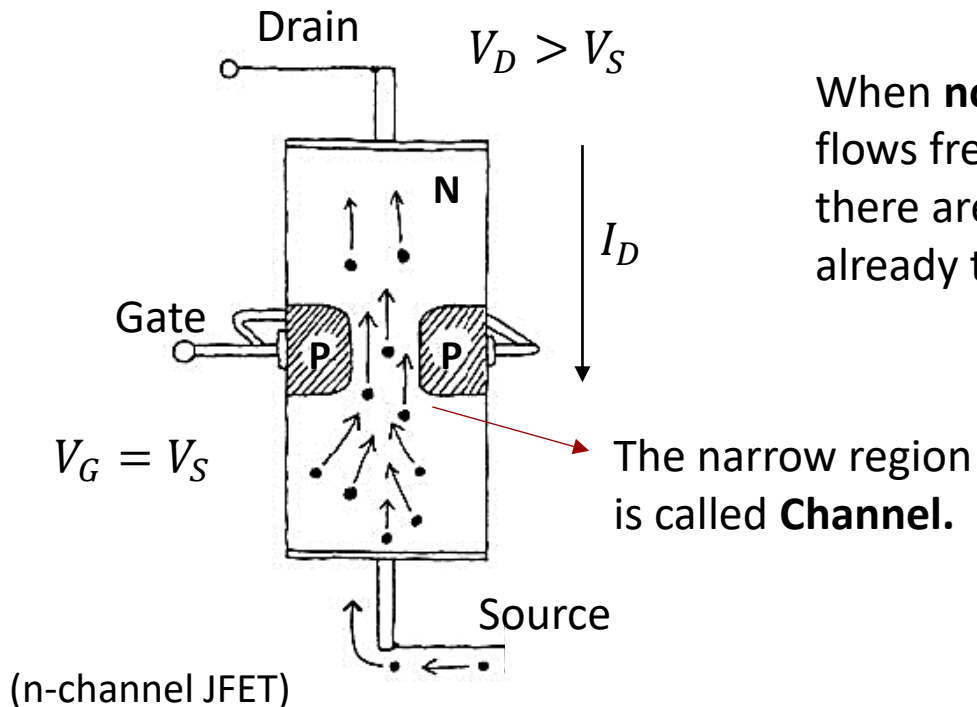
When **no voltage** is applied to the gate, current flows freely through the central n-channel (since there are a lot of negative charger carriers already there).

$V_D > V_S$

I_D

$V_G = V_S$

The narrow region is called **Channel.**
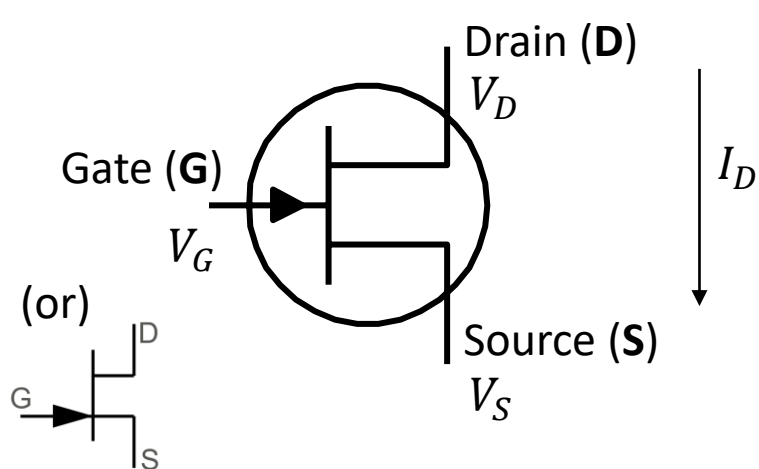
(n-channel JFET)

How a JFET Works

If the **gate** is set to a **negative voltage** relative to the source, an **electric field** is produces and the area in between the p-type semiconductor bumps and the center of the n-channel will form two reverse-biased junctions and a **depletion region** that extends into the channel. The more negative the gate voltage, the larger is the depletion region, and hence the harder it is for electrons to make it through the channel.
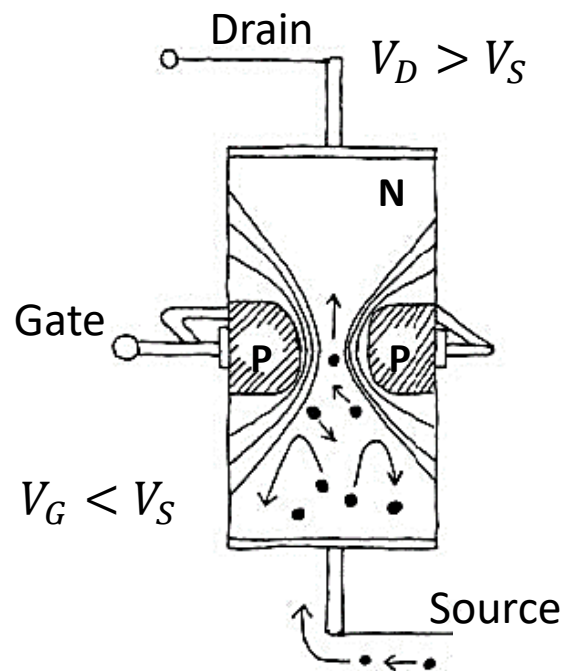
❖ For a p-channel JFET, everything is reversed!

Junction Field-Effect Transistor (JFET)

JFETs are **normally on** when there is **no voltage difference** between its gate and source leads.

Drain (**D**)
V_D
Gate (**G**)
I_D
V_G
(or)
D
G
Source (**S**)
S
V_S

Drain (**D**)
V_D
Gate (**G**)
I_D
V_G
(or)
D
G
Source (**S**)
S
V_S

With an **n-channel JFET**, if a **negative** voltage relative to source is applied to gate ($V_{GS} < 0$), the JFET becomes **more resistive to current flow** and reduces current flow from drain to source when $V_D > V_S$.

$$V_{GS} = V_G - V_S$$
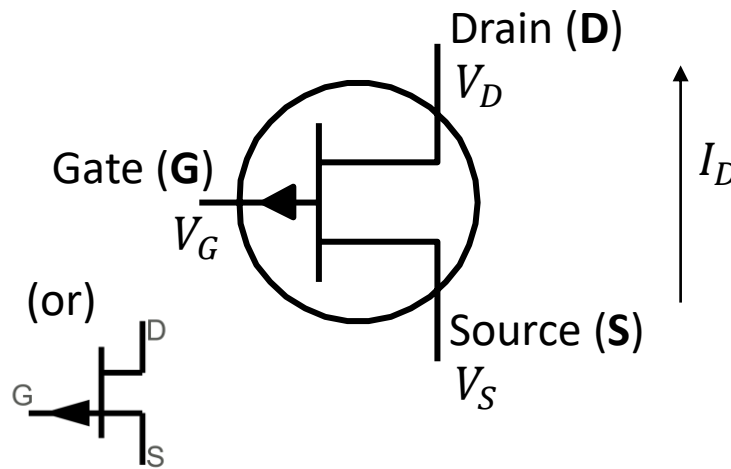
With a **p-channel JFET**, if a positive voltage relative to source is applied to gate ($V_{GS} > 0$), the JFET becomes **more resistive to current flow** and reduces current flow from source to drain when $V_S > V_D$.
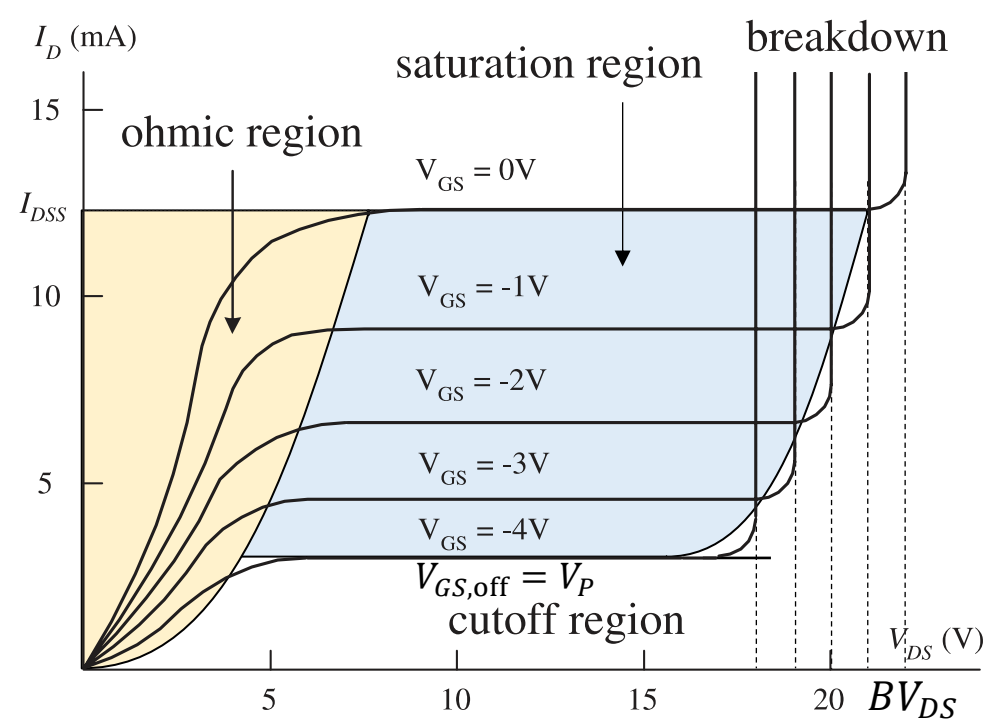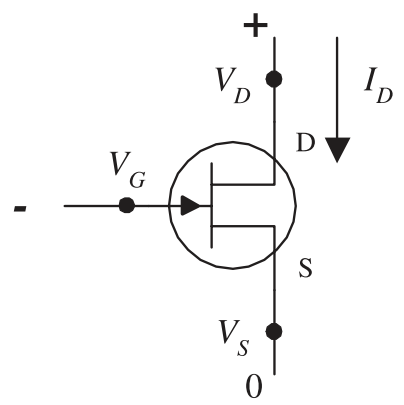
N-Channel JFET Graph

- When $V_{GS} = V_G - V_S = 0$ V, **maximum current** flows through the JFET. This current is called steady-state drain current for zero bias (I_{DSS}) which is **constant** for a JFET.

- When V_{DS} is small, the drain current I_D varies nearly linearly with V_{DS}. This region is called the **ohmic** or **linear region** and the JFET behaves like a **voltage-controlled resistor**.

- The section of the graph where the curves flatten out is called the **active** or **saturation region**, and the drain current I_D is strongly influenced by V_{GS} but hardly at all influenced by $V_{DS} = V_D - V_S$.
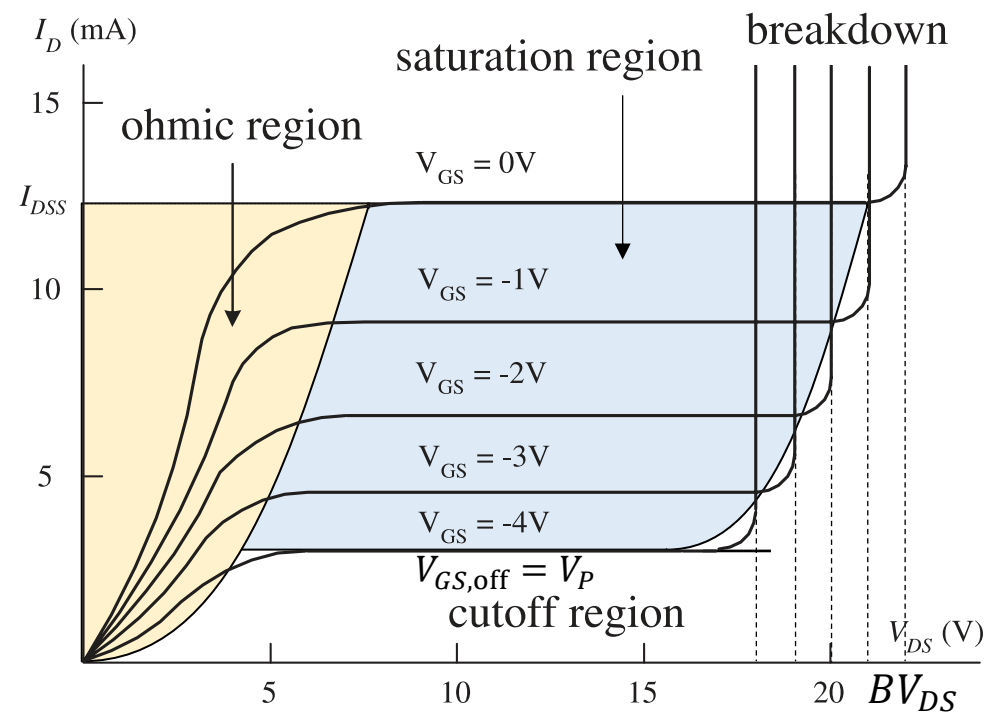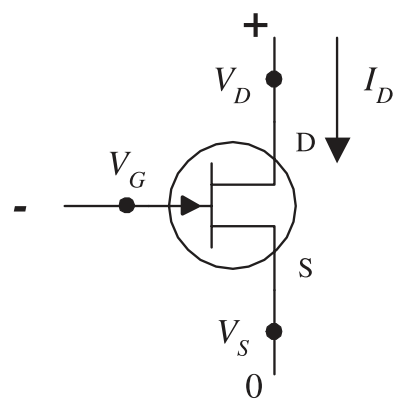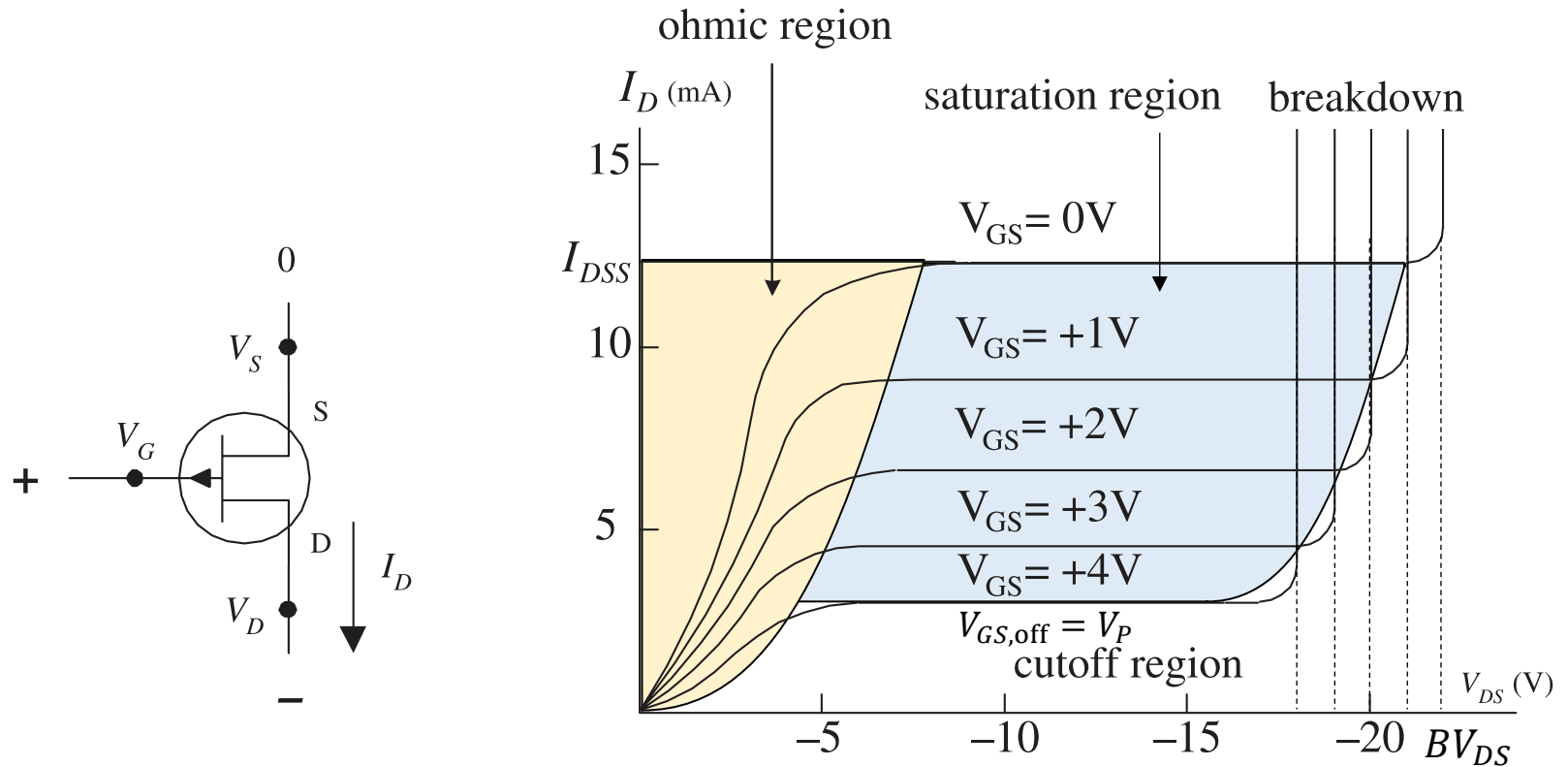
N-Channel JFET Graph

- $V_{GS,\text{off}}$ is the particular V_{GS} voltage that causes the JFET to **turn off** (practically no current flows through device and the JFET behaves like an open circuit) is called the **cutoff voltage** (or **pinch-off voltage** V_P).

- When V_{DS} increases, I_D increases extremely and the **JFET loses its ability to resist current**. This effect is called **drain-source breakdown**, and its voltage is expressed as BV_{DS}.
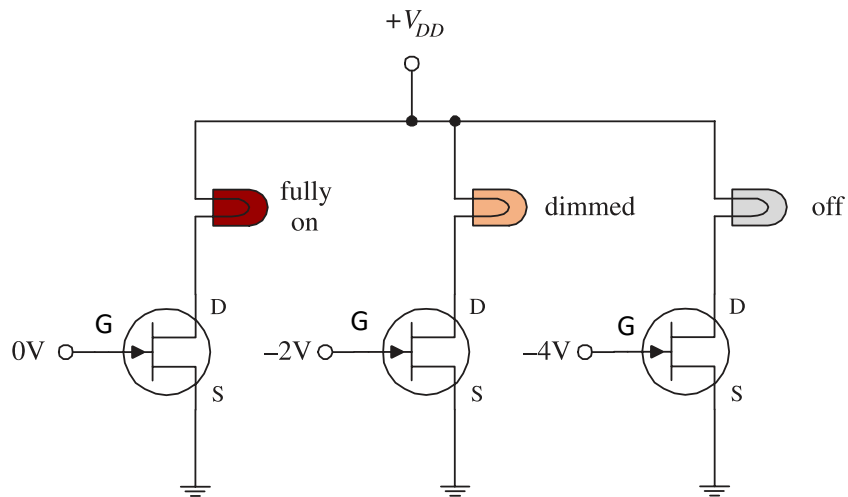
P-Channel JFET Graph

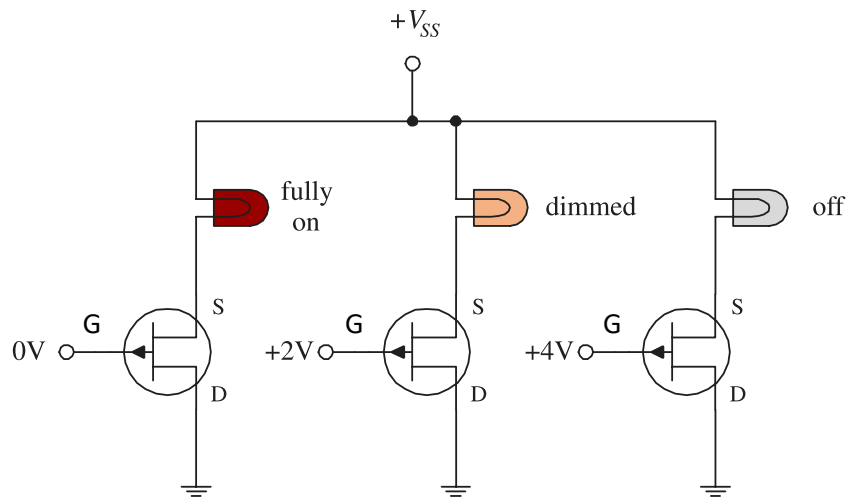Similar explanations for P-Channel JFET Graph:

# Application: Basic Operation - Light Dimmer

n-channel JFET

p-channel JFET

In the **n-channel** circuit, a more negative gate voltage causes a larger drain-to-source resistance, hence causing the light bulb to receive less current. In the **p-channel** circuit, a more positive gate voltage causes a greater source-to-drain resistance.

Application: Basic Current Source

❶

$+V_{DD}$

I_D R_{load}

G   D

S

❷

I_D(mA)

I_{DSS}

-4   -3   -2   -1   0 V_{GS} (V)

$+V_{DD}$

I_D R_{load}

G   D

S

R_S
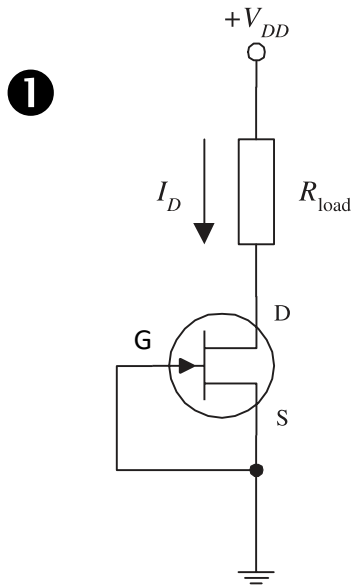
A simple current source can be constructed by shorting the source and gate terminals together (self-biasing, $V_{GS} = 0$ V). Hence, the drain current is simply equal to I_{DSS}.
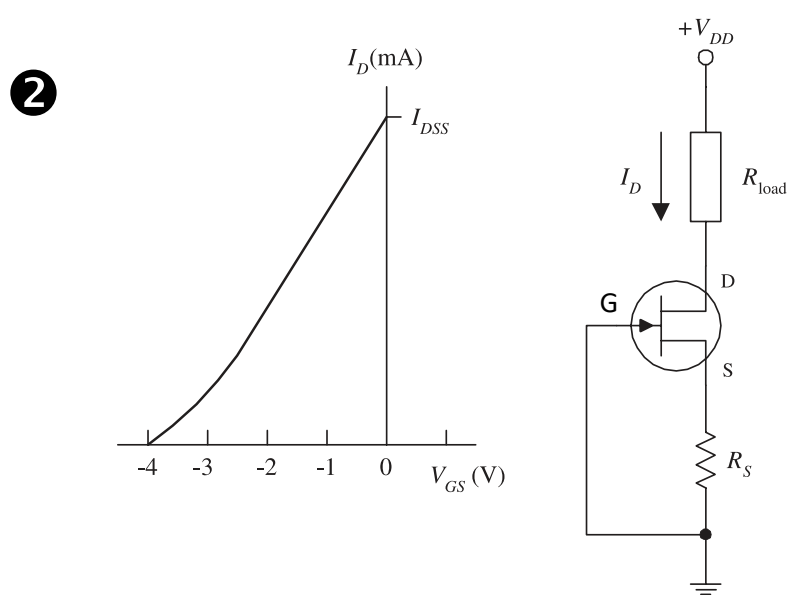
If you place a resistor between the source and ground, you can make the current source **adjustable**. By increasing R_S, you can decrease I_D.

Note: These simple JFET current sources are not as stable as a good bipolar or op amp current source.

Metal-Oxide-Semiconductor FET (MOSFET)

Metal-Oxide-Semiconductor FET (MOSFET)

Metal-Oxide-Semiconductor Field-Effect Transistors (**MOSFETs**) are the **most popular** transistors used today that in some ways resemble JFETs. When a small voltage is applied at its gate lead, the current flow through its drain-source channel is altered. However, unlike JFETS, MOSFETs have **larger** gate lead **input impedances** ($\geq 10^{14}$ vs 10^{10} Ω), which means that they draw almost no gate current at all. This is because of **a thin silicon dioxide layer insulating** the gate from the **substrate** (drain-source channel).

The two major kinds of MOSFETs are **depletion-type** MOSFETs and **enhancement-type** MOSFETs. Each type comes in either **n-channel** or **p-channel** forms.
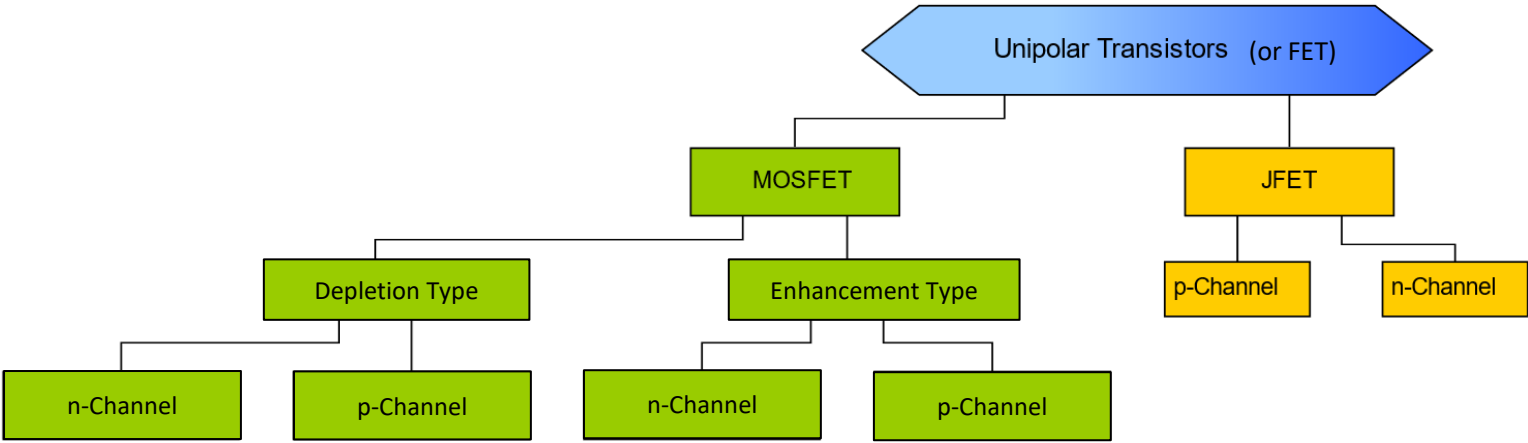
How a Depletion-Type MOSFET Works

A **depletion-type** MOSFET is **normally on** or **normally conductive** (maximum current flows from drain to source) when $V_{GS} = 0$ V. However, if a voltage is applied to its gate lead ($V_G < V_S$ for n-channel and $V_G > V_S$ for a p-channel), the drain-source channel becomes **more resistive** (**similar to a JFET**).

In an n-channel depletion-type MOSFET, charge carriers (electrons) are already present within the n-type. If a negative gate-source voltage is applied, the resulting **electrical field** acts to cutoff the flow of electrons through the channel.
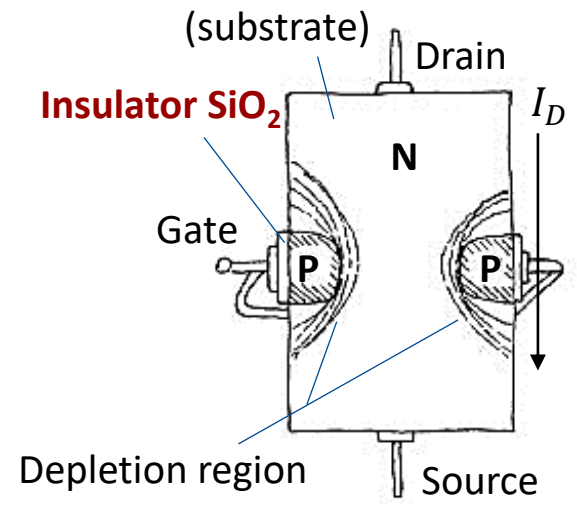
❖ For a p-channel depletion-type MOSFET, everything is reversed!

How an Enhancement-Type MOSFET Works

An **enhancement-type** MOSFET is **normally off** or **normally resistive** (minimum current flows from drain to source) when $V_{GS} = 0$ V. However, if a voltage is applied to its gate lead ($V_G > V_S$ for n-channel and $V_G < V_S$ for a p-channel), the drain-source channel becomes **less resistive**.

An n-channel enhancement-type MOSFET have few charge carriers within it. If a positive gate-source voltage is applied, an **electric field** formed in the substrate below the gate **repels holes in the p-type substrate** and **electrons** which are **minor charge carriers** within the p-type semiconductor region **migrate into the channel** between two n-type semiconductors and thereby **increase the conductance** of the channel.
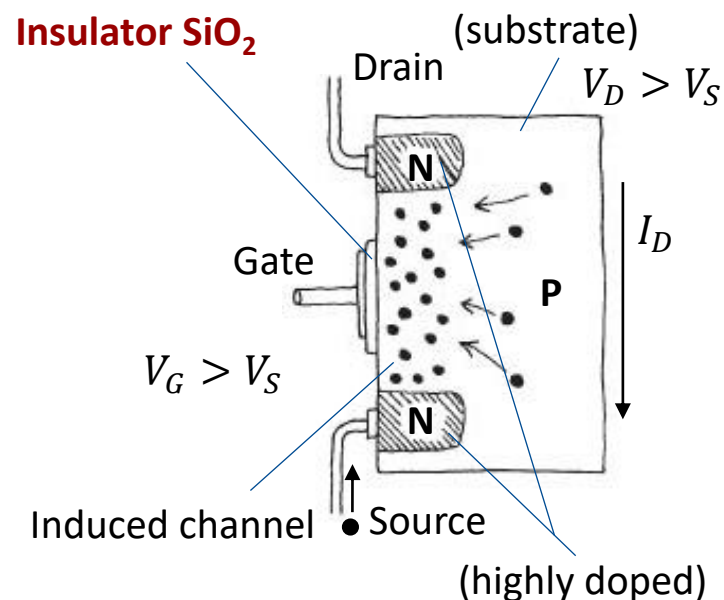

Note: Graphs and definitions of maximum current I_{DSS}, ohmic or linear region, active or saturation region, cutoff voltage, and drain-source breakdown for MOSFETs are similar to JFETs.

Stony Brook University

MOSFET Symbols

- The direction of the gate or substrate **arrow** distinguishes between p-channel (arrow out) and n-channel (arrow in).
- A **separation** is shown between the gate and source in the MOSFET but not in the JFET.
- A **broken line** between the source and drain indicates an enhancement-mode device in contrast to a solid line for a depletion-mode device.
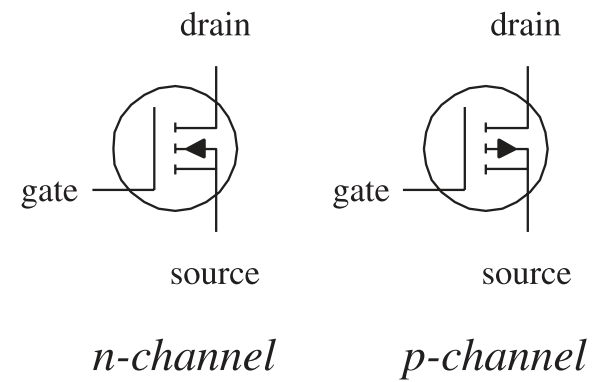- The gate line is usually **offset** toward the source, so the source side can be easily identified.
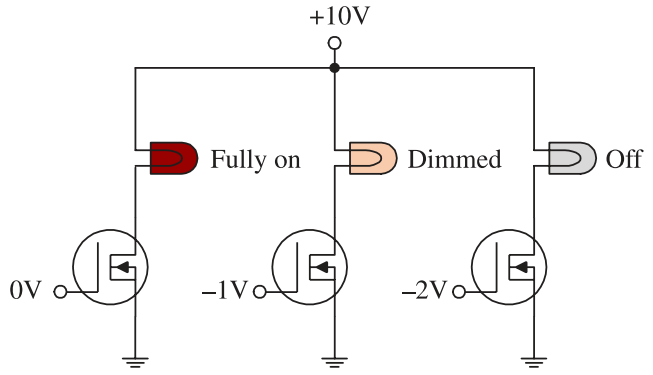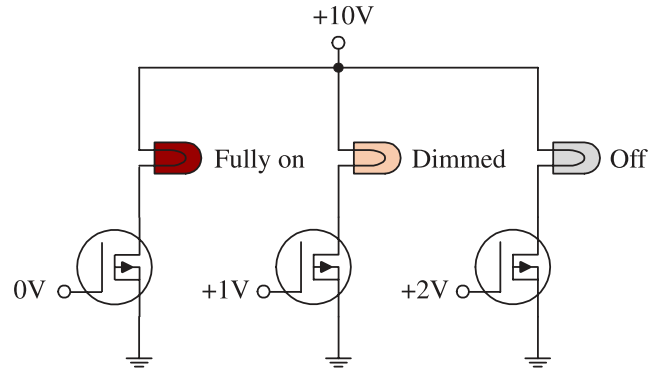

JFET
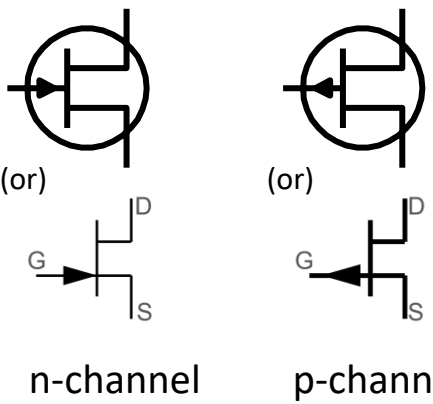
(or)

n-channel   p-channel

Depletion MOSFETs
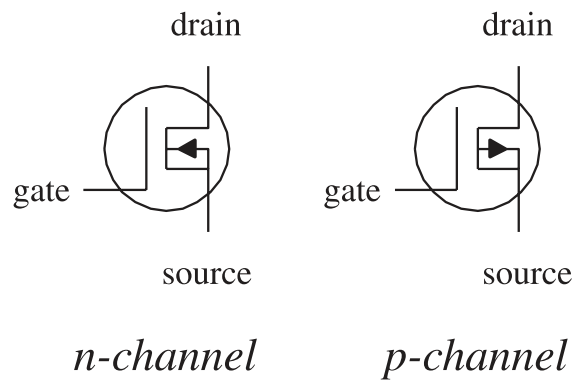
n-channel   *p-channel*

Enhancement MOSFETs

n-channel   *p-channel*

Application: Basic Operation - Light Dimmer
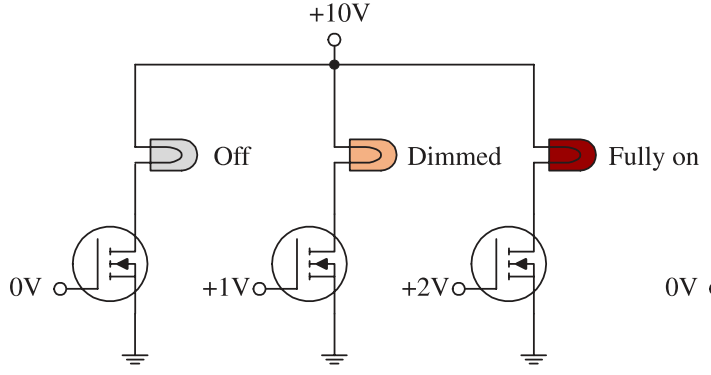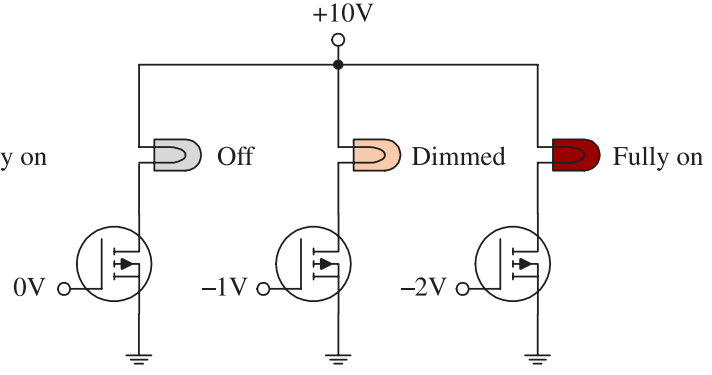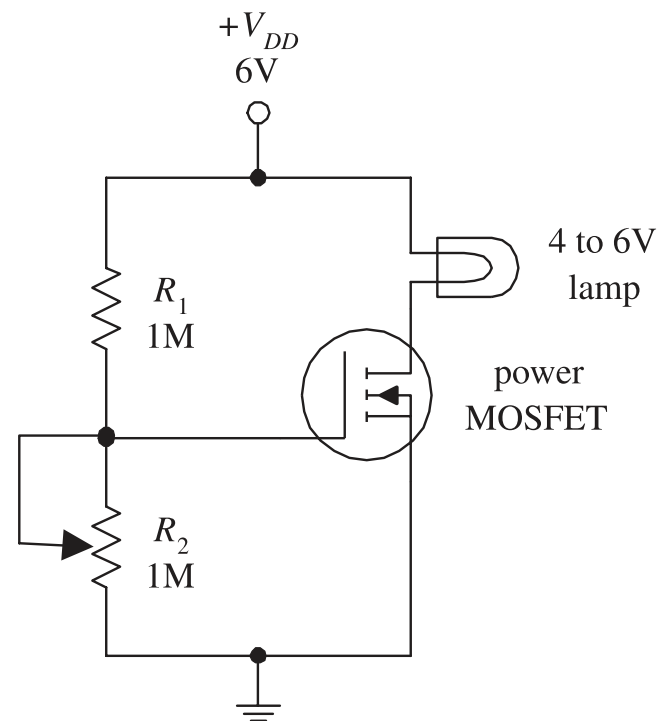
Application: Light Dimmer

Here, an n-channel enhancement-type power MOSFET is used to **control the current** flow through a lamp. The voltage-divider resistor R_2 **sets the gate voltage**, which in turn **sets the drain current** through the lamp.

Application: Switch

The MOSFET is a good choice to use as a digital-to-analog interface; its extremely high input resistance and low input current make it a good choice for powering high-voltage or high-current analog circuits **without** worrying about **drawing current** from the driving logic.

- The 10 kΩ is pull-down resistor is used to keep MOSFET off and protect from electrostatic voltage which may cause the MOSFET turns on occasionally.
- 100 Ω gives protection to the logic pin.
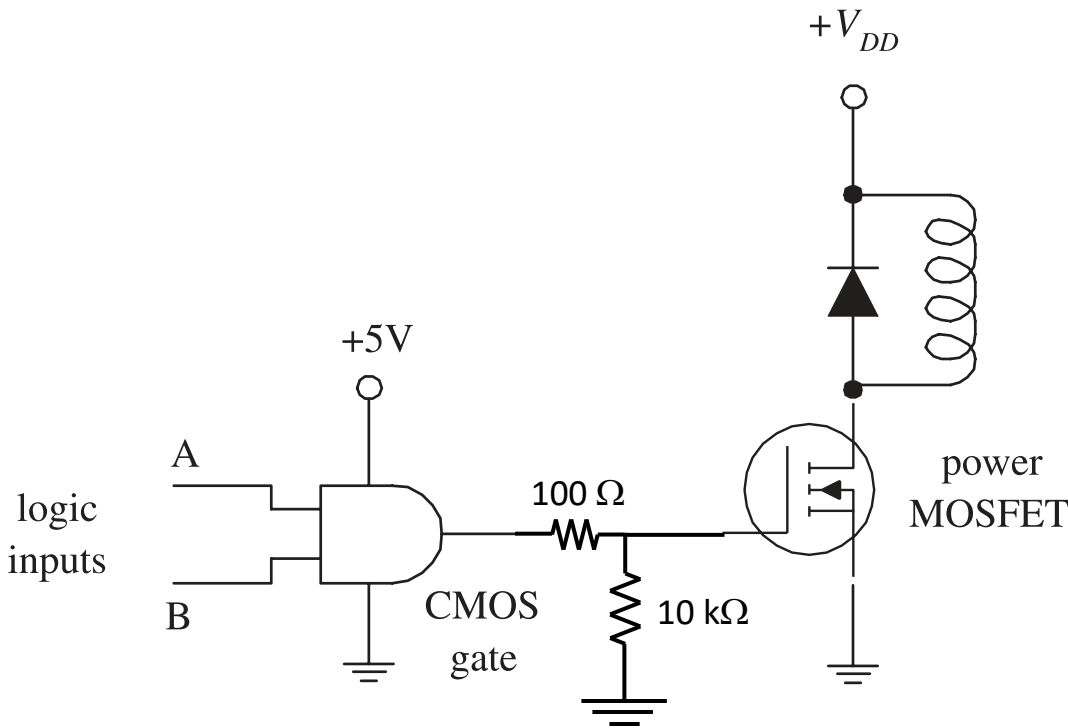
BJT and FET

Both BJTs and FETs operate by **controlling current between two terminals** using a **voltage** applied to a third terminal. However, BJTs require a biasing input (or output) **current** at their control leads, whereas FETs require **only a voltage** (practically no current) to conduct the charge carriers.

Advantages of FETs:

- Drawing little or **no input (or output) current** at their control leads, which results in high input impedance ($\geq 10^{10}$ Ω); i.e., in contrast with BJTs, the FET's control lead will not have much influence on the current dynamics of the control circuit,
- **Easier and cheaper** to manufacture,
- Can be made **extremely small** (FETs are important components in design of digital ICs),
- Generally, much **less noisy** than the BJTs.

Integrated Circuits

Integrated Circuit

An **Integrated Circuit** (**IC**) is a miniaturized circuit that contains a number of resistors, capacitors, diodes, and transistors stuffed together on a single small chip of silicon. The number of resistors, capacitors, diodes, and transistors within an IC may vary from just a few to millions.

The trick is to make **all the components** out of tiny **n-type** and **p-type silicon** structures that are embedded into the **silicon chip** during the production phase. To connect the little transistors, resistors, capacitors, and diodes together, **aluminum** plating is applied along the surface of the chip.
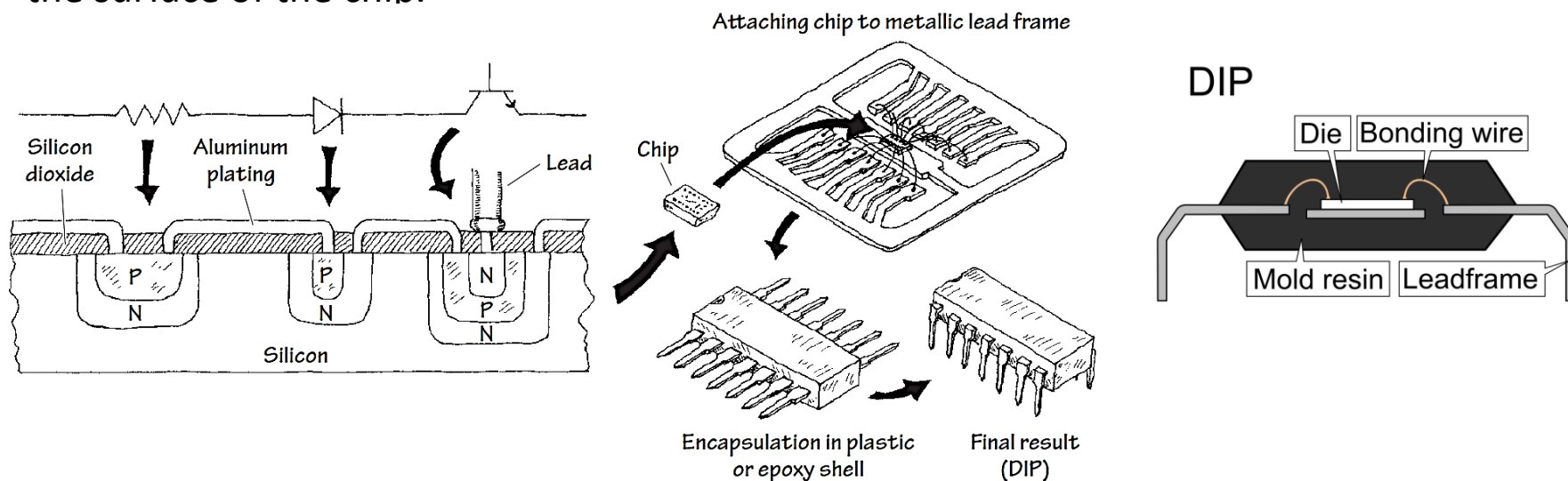
ICs Forms

ICs come in **Analog**, **Digital**, or **Analog/Digital** form:

❖ **Analog ICs** produce, amplify, or respond to varying voltages (e.g., voltage regulators, operational amplifiers, comparators, timers, and oscillators).

❖ **Digital ICs** respond to or produce signals having only high and low voltage states (e.g., logic gates such as AND, OR, or NOR, microcontrollers, memories, binary counters, shift registers, multiplexers, encoders, and decoders).

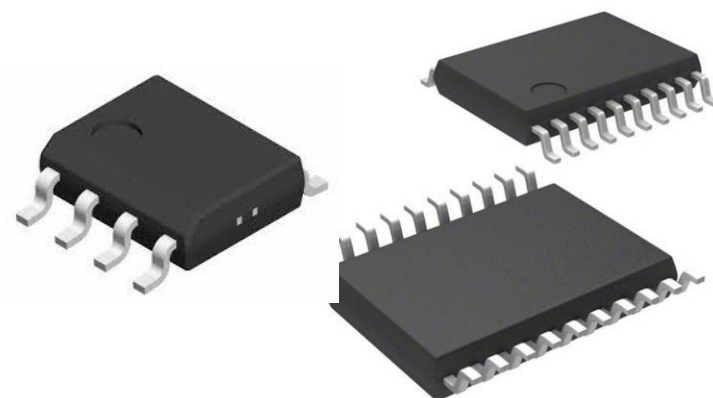❖ **Analog/Digital ICs** share properties common with both analog and digital ICs.
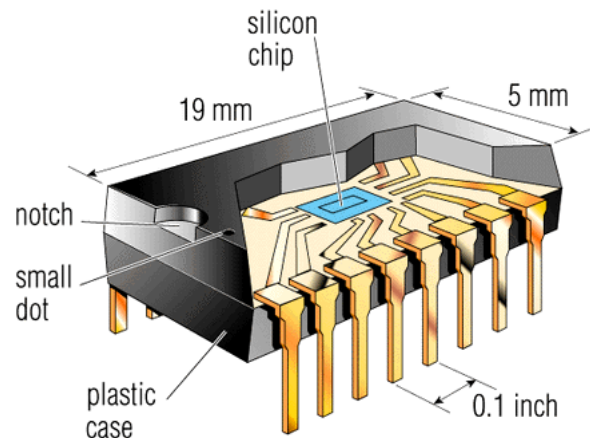
The Most Common IC Packages

The determining factors for the **package type** are the **number of pins** and the **power dissipation**.

1. Dual In-Line Package (**DIP** or **DIL**)

DIP Socket

notch

1   8
2   7
3   6
4   5
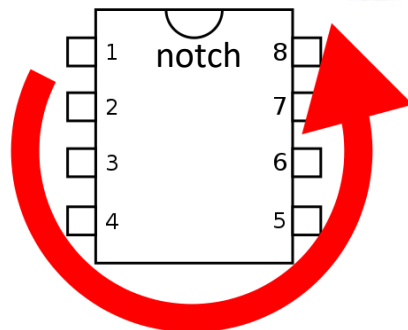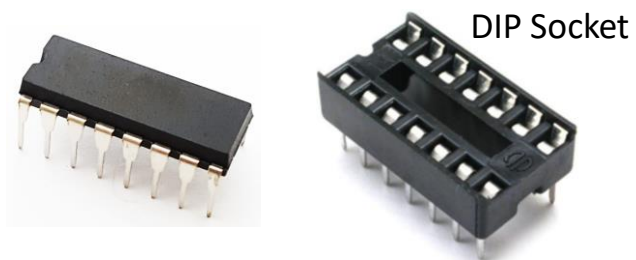
2. Small Outline Integrated Circuit (**SOIC**) or **SO** [a surface-mounted IC]

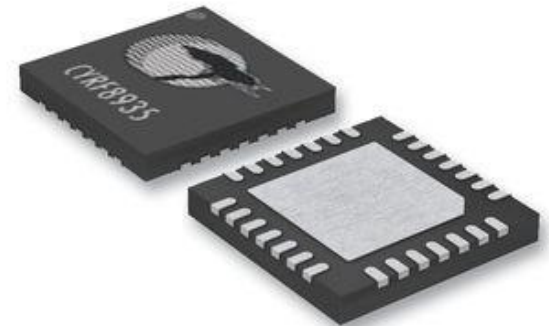Variants: SOP, SSOP, MSOP, TSOP, TSSOP

The Most Common IC Packages

3. Quad Flat Package (QFP)

(TQFP: Thin quad flat pack)

4. Quad-Flat No-Leads (QFN)

(TQFN: Thin quad flat no leads)

- Many of these IC packages are not really made for hand soldering.

- You will often find that the same ICs are available in **multiple packages**, making it possible to prototype in something easy to solder like DIP or SO, and then switch to a smaller package for the final product.

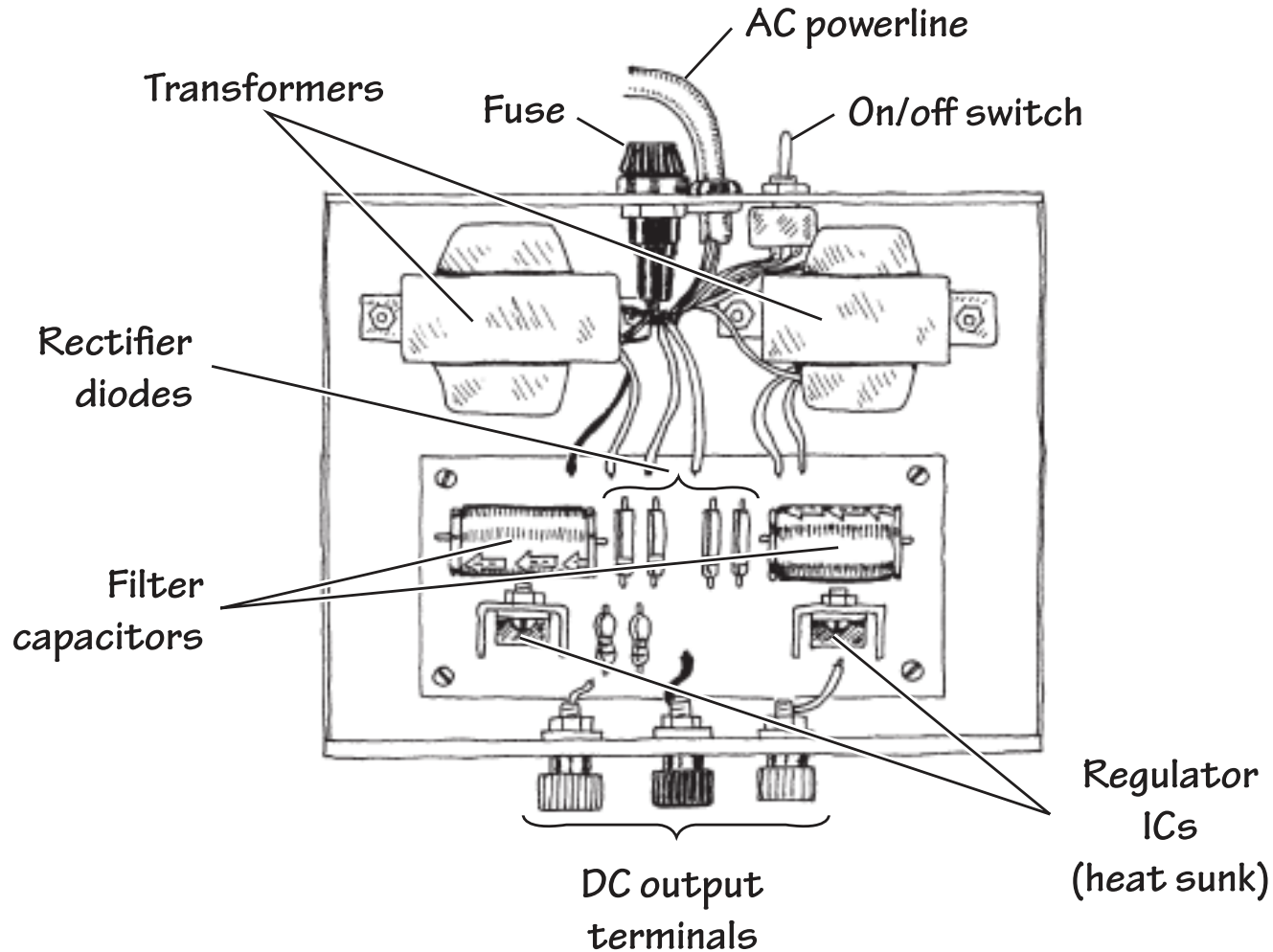| PACKAGE	PITCH (mm)
DIP	2.54
SO/SOIC/SOP	1.27
MSOP/SSOP	0.65
SOT	0.65
TQFP	0.8
TQFN	0.4-0.65

Voltage Regulators

Converting AC Voltage into a Lower-Level DC Voltage
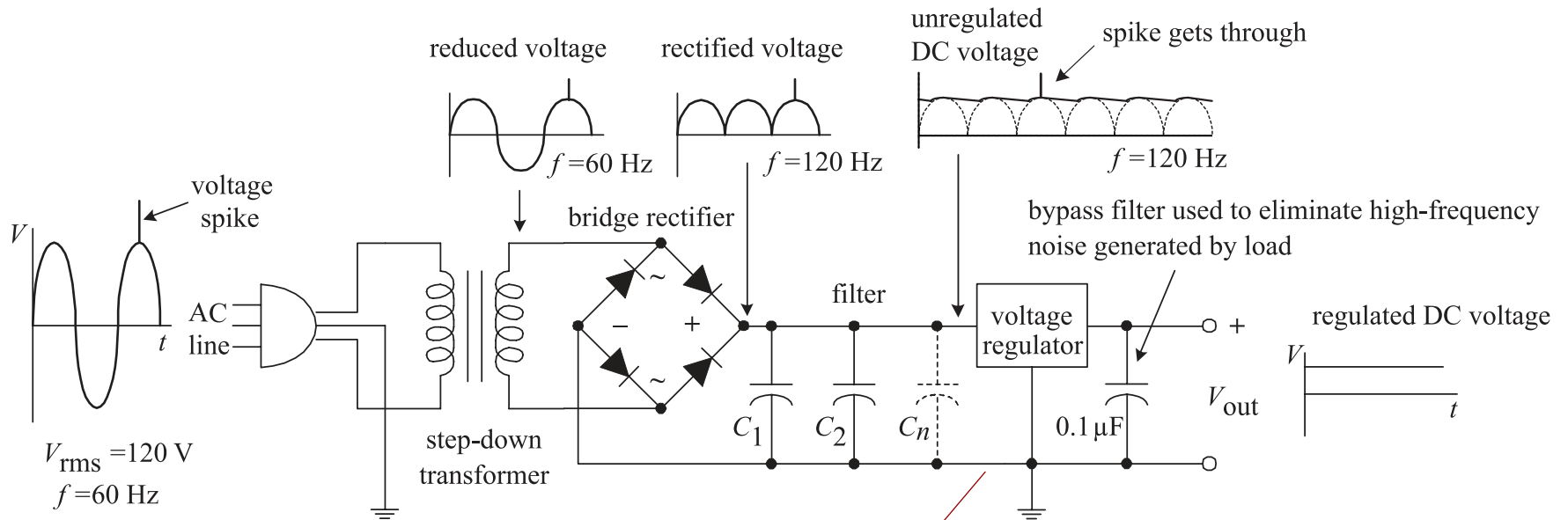
Problems of Unregulated Voltage:

- If there are any **sudden surges** within the AC input voltage (spikes, dips, etc.), these variations will be expressed at the supply's output which is **not good for sensitive circuits** (e.g., digital IC circuits).
- If a highly resistive (low-current) load is replaced with a lower-resistance (high-current) load, the unregulated output **voltage will drop**.

DC Power Supply

Transformers

AC powerline

Fuse

On/off switch

Rectifier
diodes

Filter
capacitors

Regulator
ICs
(heat sunk)

DC output
terminals

Voltage Regulators

Although the **Zener diode** voltage regulator is cheap and simple to use, it has some drawbacks:
- The output voltage cannot be set to a precise value,
- Regulation against source ripple and changes in load is limited.

Voltage Regulator is an IC designed to eliminate the **spikes** and maintain a **constant** output voltage with load variations.

This IC automatically adjust the amount of **current** flowing through a load (so as to maintain a constant output voltage) by comparing the supply's DC output with a fixed or programmed internal reference voltage.
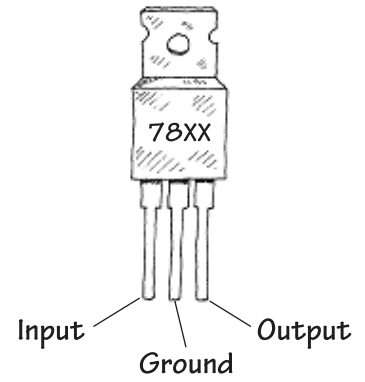
Voltage-Regulator IC $(V_{\text{out}} < V_{\text{in}})$
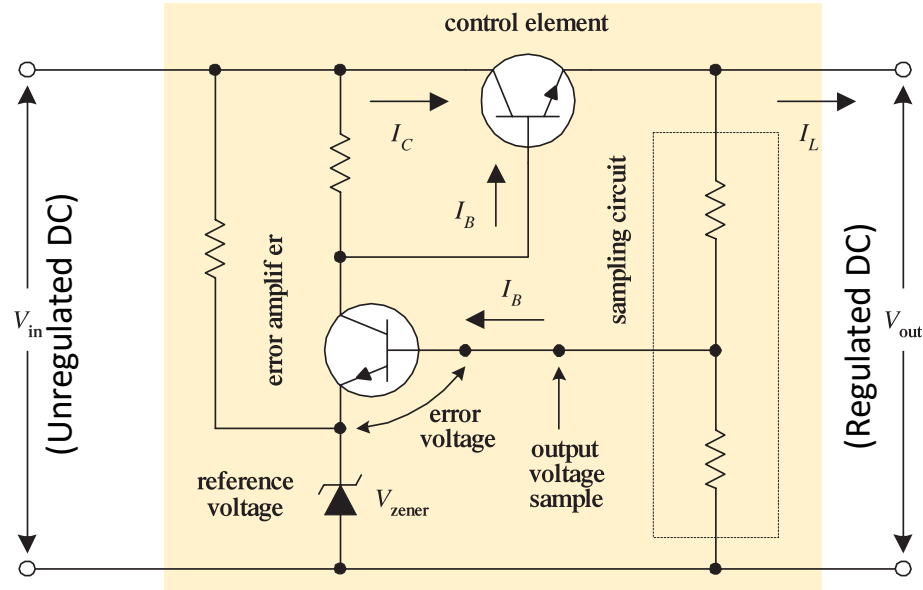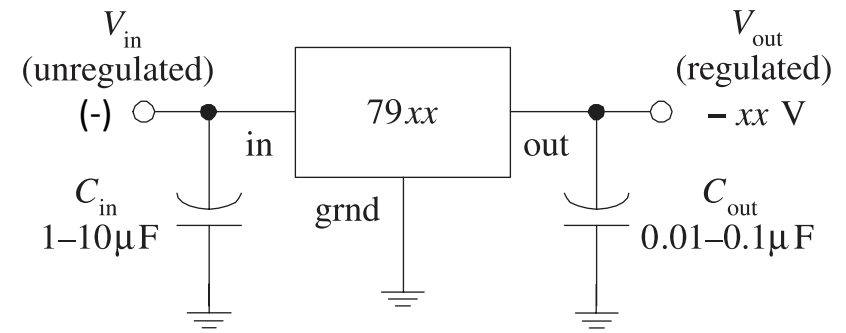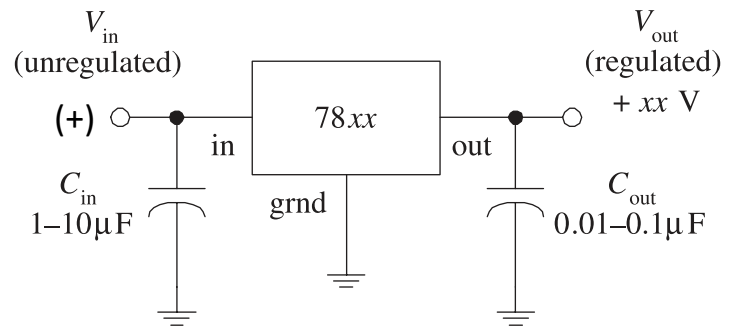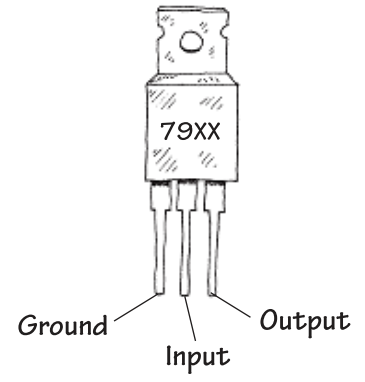
Fixed-Regulator ICs

LM78xx and LM79xx are popular **fixed-regulator** ICs. The "xx" digits represent the output voltage, e.g., 7805 (5 V), 7812 (12 V), etc. These devices can handle a maximum output current of 1.5 A by using a proper heat-sink.
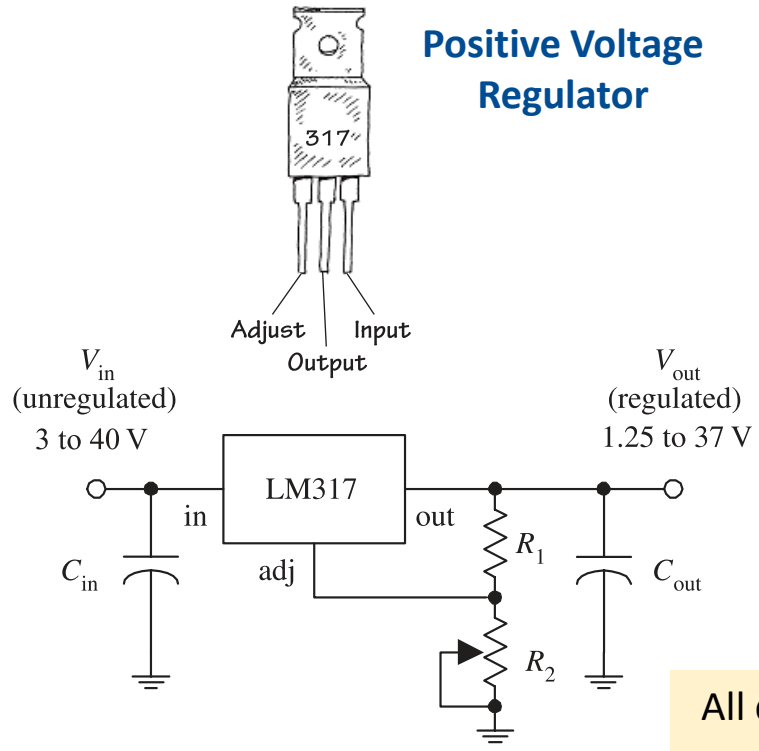
Positive Voltage Regulator

- V_{in} should be at least 2 V higher than V_{out} (smaller difference $\Rightarrow$ less energy dissipation).
- All capacitors are used to remove unwanted input or output spikes/noise.

Negative Voltage Regulator
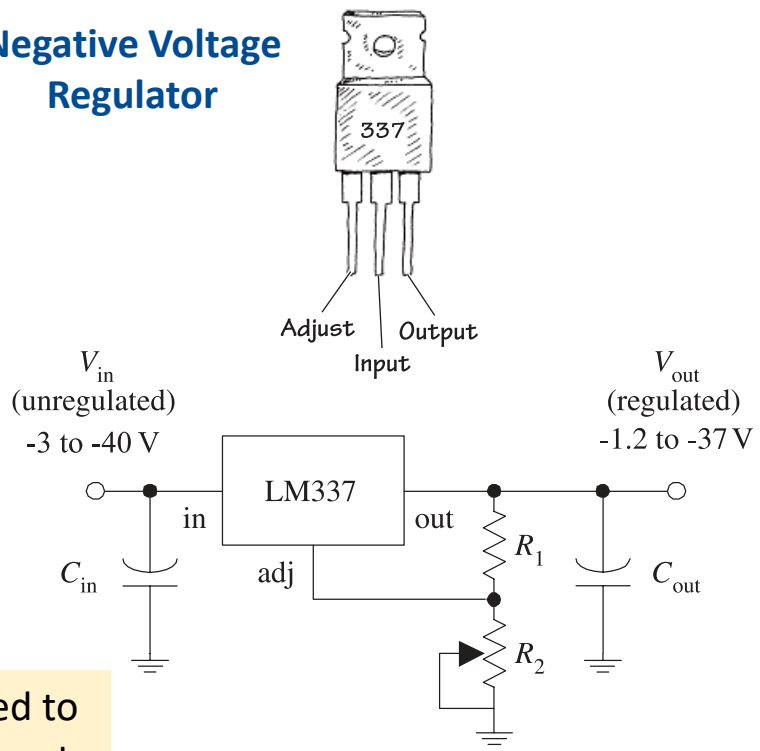
FETs: JFET
○○○○○○○○○○

FETs: MOSFET
○○○○○○○○

Integrated Circuits
○○○○

Voltage Regulators
○○○○●

Adjustable-Regulator ICs

LM317 and LM337 are popular **adjustable-regulator** ICs for providing different voltages.

Positive Voltage Regulator

Negative Voltage Regulator

V_{in}
(unregulated)
3 to 40 V

LM317

V_{out}
(regulated)
1.25 to 37 V

in | out
adj

C_{in} | R_1 | C_{out}
R_2

V_{in}
(unregulated)
-3 to -40 V

LM337

V_{out}
(regulated)
-1.2 to -37 V

in | out
adj

C_{in} | R_1 | C_{out}
R_2

All capacitors are used to remove unwanted input or output spikes/noise (0.1μF or larger)

$$V_{\text{out}} = 1.25\text{V} \left(1 + \frac{R_2}{R_1}\right)$$

$$V_{\text{out}} = -1.25\text{V} \left(1 + \frac{R_2}{R_1}\right)$$